CLAIMS

1. A DC/AC converter circuit for controllably delivering power to a load, comprising an input voltage source; a first plurality of overlapping switches and a second plurality of overlapping switches being selectively coupled to said voltage source, said first plurality of switches defining a first conduction path, said second plurality of switches defining a second conduction path; a pulse generator generating a pulse signal; drive circuitry receiving said pulse signal and for controlling a conduction state of said first and second plurality of switches; a transformer having a primary side and a secondary side, said primary side selectively coupled to said voltage source in an alternating fashion through said first conduction path and, alternately, through said second conduction path; a load coupled to said secondary side of said transformer; and a feedback loop circuit between said load and said drive circuitry supplying a feedback signal indicative of power being supplied to said load; wherein, said drive circuitry alternating the conduction state of said first and second plurality of switches, controlling the overlap time of the switches in the first plurality of switches, and controlling the overlap time of the switches in the second plurality of switches, to couple said voltage source to said primary side based at least in part on said feedback signal and said pulse signal.

2. A circuit as claimed in claim 1, wherein said input voltage source comprises a DC voltage.

3. A circuit as claimed in claim 1, wherein said drive circuitry generating:

a first complimentary pulse signal from said pulse signal; and

a ramp signal;

wherein said pulse signal being supplied to a first one of said first plurality of switches to control the conduction state thereof, said ramp signal being compared with at least said feedback

signal to generate a second pulse signal, said second pulse signal being supplied to a second one of said first plurality of switches and controlling the conduction state thereof, wherein a controllable overlap condition exists between the conduction state of said first and second switches of said first plurality of switches; said drive circuitry further generating a second complimentary pulse signal based on said second pulse signal; wherein said first and second complimentary pulse signals controlling the conduction state of a first and second ones of said second plurality of switches, respectively, wherein a controllable overlap condition exists between the conduction state of said first and second switches of said second plurality of switches.

4. A circuit as claimed in claim 3, wherein said first and second plurality of switches comprising MOSFET transistors.

5. A circuit as claimed in claim 4, wherein each said transistor further comprising an intrinsic switch in parallel with each transistor in reverse bias with respect to said voltage source, each said intrinsic switch for bleeding off energy stored within said primary side of said transformer by completing a conduction path between said voltage source and said primary side when said transistors are in a nonconducting state.

6. A circuit as claimed in claim 5, wherein said intrinsic switch comprises a diode.

7. A circuit as claimed in claim 3, wherein a phase difference between said pulse signal and said first complimentary pulse signal is approximately 180 degrees; a phase difference between said second pulse signal and said second complimentary pulse signal is approximately 180 degrees, so that a short circuit condition does not exists between said first conduction path and said second conduction path.

8. A circuit as claimed in claim 7, wherein the conduction state of said first plurality of switches and said second plurality of switches determining the power delivered to said load.

9. A circuit as claimed in claim 3, wherein said feedback control loop comprising a first comparator for comparing a reference signal with said feedback signal and producing a first output signal, and a second comparator for comparing said first output signal with said ramp signal and producing said second pulse signal based on the intersection of said first output signal and said ramp signal.

10. A circuit as claimed in claim 9, wherein said load feedback signal being a measure of the current flowing through said load.

11. A circuit as claimed in claim 9, further comprising a current sense circuit receiving said feedback signal and generating a trigger signal; said feedback loop circuit further comprising a switch circuit between said first and second comparator, said switch circuit receiving said trigger signal and generating either said first output signal or a predetermined minimum signal, based on the value of said trigger signal.

12. A circuit as claimed in claim 9, wherein said reference signal being generated by a reference signal generator, and being indicative of a desired power delivered to said load.

13. A circuit as claimed in claim 9, further comprising an overcurrent protection circuit receiving said feedback signal and controlling said pulse generator based on the value of said feedback signal; and an overvoltage protection circuit receiving a voltage signal from across said load and said first output signal and comparing voltage signal from across said load and said first output signal, and controlling said pulse generator based on the value of said voltage signal from across said load.

14. A circuit as claimed in claim 1, wherein said pulse generator comprising a programmable pulse frequency generator circuit and being programmed to initiate said converter circuit with a pulse frequency having a 50% duty cycle and starting with a predetermined frequency, and sweeping said frequency downward at a predetermined rate and at predetermined steps.

15. A circuit as claimed in claim 1, wherein said load comprises one or more cold cathode fluorescent lamps (CCFLs).

16. A circuit as claimed in claim 1, wherein said primary side comprising a resonant tank circuit comprising an inductor and a capacitor.

17. A circuit as claimed in claim 1, wherein said secondary side comprising a voltage divider circuit in parallel with an inductor in parallel with said load.

18. A converter circuit for delivering power to a CCFL load, comprising:

a voltage source;

a transformer having a primary side and a secondary side;

a first pair of switches and a second pair of switches defining a first and second conduction path, respectively, between said voltage source and said primary side;

a CCFL load circuit coupled to said secondary side;

a pulse generator generating a pulse signal;

a feedback circuit coupled to said load generating a feedback signal; and

drive circuitry receiving said pulse signal and said feedback signal and coupling said first pair of switches or said second pair of switches to said voltage source and said primary side based on said pulse signal and said feedback signal to deliver power to said load.

19. A circuit as claimed in claim 18, wherein said pulse signal having a predetermined frequency; said drive circuitry comprising a first, second, third and fourth drive circuits; said first

pair of switches comprising first and second transistors, said second pair of switches comprising third and fourth transistors; said first, second, third and fourth drive circuits connected to the control lines of said first, second, third and fourth transistors, respectively; said pulse signal supplied to said first drive circuit so that said first transistor is switched in accordance with said pulse signal, said third drive circuit generating a first complimentary pulse signal and a ramp signal based on said drive signal and supplying said first complimentary pulse signal to said third transistor so that said third transistor is switched in accordance with said first complimentary pulse signal; said ramp signal and said feedback signal being compared to generate a second pulse signal, said second pulse signal being supplied to said second drive circuit so that said second transistor is switched in accordance with said second pulse signal; said fourth driving circuit generating a second complementary pulse signal based on said second pulse signal and supplying said second complementary pulse signal to said fourth transistor so that said fourth transistor is switched in accordance with said second complimentary pulse signal; wherein the simultaneous conduction of said first and second transistors, and said third and fourth transistors, respectively, controls the amount of power delivered to said load.

20. A circuit as claimed in claim 18, wherein said pulse signal and first complementary pulse signal being approximately 180^0 out of phase, said second pulse signal and said second complementary signal being approximately 180^0 out of phase, and said pulse signal and said second pulse signal being controlled to deliver power along said first conduction path, and said first complementary signal and said second complementary signal being controlled to deliver power along said second conduction path.

21. A circuit as claimed in claim 19, wherein said feedback circuit comprises a first comparator for comparing said feedback signal with a reference signal and generating a first

output signal; and a second comparator for comparing said first output signal with said ramp signal and generating said second pulse signal based on the intersection between said ramp signal and said first output signal.

22. A circuit as claimed in claim 21, wherein said reference signal being generated by a reference voltage generator, and being indicative of a desired power value to be delivered to said load.

23. A circuit as claimed in claim 21, further comprising an overvoltage protection circuit coupled to said load and said pulse generator, said overvoltage protection circuit receiving as input the voltage across said load and controlling said pulse generator based on said on the value of said voltage across said load.

24. A circuit as claimed in claim 23, wherein said overvoltage protection circuit comprises a comparator for comparing said voltage signal across said load and said first output signal and generating a control signal to said pulse generator to control the power delivered by said pulse generator.

25. A circuit as claimed in claim 24, wherein said overvoltage protection circuit further comprises a timer circuit wherein said control signal being controlled by a predetermined time generated by said timer circuit.

26. A circuit as claimed in claim 21, further comprising an overcurrent protection circuit coupled to said pulse generator and receiving as input said feedback signal, and controlling said pulse generator based on the value of said feedback signal.

27. A circuit as claimed in claim 19, wherein said first and third transistors being coupled together is series with each other and in parallel with said voltage source and said primary side,

said second and fourth transistors being coupled together in series with each other and in parallel with said voltage source and said primary side.

28. A circuit as claimed in claim 19, further comprising an intrinsic switch in parallel with each said transistor, said intrinsic switch permitting energy to flow from said primary side through said first or second conduction path before each said transistor is switched to conduct.

29. A circuit as claimed in claim 18, wherein said primary side defining a resonant tank circuit having a single resonant operating frequency.

30. A circuit as claimed in claim 19, wherein said first and third drive circuits comprise a totem pole circuit, and said second and fourth drive circuits are selected from the group consisting of: a boot strap circuit, a high-side drive circuit or a level shifting circuit.

31. A circuit as claimed in claim 19, wherein said second and fourth drive circuits further comprising an inverter for generating said first and second complementary pulse signals, respectively.

32. A circuit as claimed in claim 31, wherein said second drive circuit further comprises a sawtooth generating circuit for generating said ramp signal, said sawtooth signal having a frequency matching said pulse signal.

33. A circuit as claimed in claim 21, further comprising a flip-flop circuit coupled to said second pulse signal and supplying said second pulse signal to said second drive only when said third transistor is switched into a conducting state.

34. A circuit as claimed in claim 18, further comprising a phase-lock loop (PLL) circuit having a first input signal from said primary side and a second input signal using said feedback signal, said PLL circuit sending a control signal to said pulse generator for controlling a pulse width of said pulse signal based on the phase difference between said first and second inputs.

35. A method for controlling a zero-voltage switching circuit to deliver power to a load, said method comprising the steps of:

supplying a DC voltage source;

coupling a first and second transistor defining a first conduction path and a third and fourth transistor defining a second conduction path to said voltage source and a primary side of a transformer

generating a pulse signal to having a predetermined pulse width;

coupling a load to a secondary side of said transformer;

generating a feedback signal from said load; and

controlling said feedback signal and said pulse signal to determine the conduction state of said first, second, third and fourth transistors.

36. A method as claimed in claim 35, further comprising the step of timing the conduction of said transistors so that said first and third transistors do not conduct simultaneously, and said second and fourth transistors do not conduct simultaneously.

37. A method as claimed in claim 35, further comprising the steps of:

generating a first and second complementary signals;

generating a ramp signal;

comparing said ramp signal to said feedback signal and generating a second pulse signal;

supplying said pulse signal to said first transistor to control the conduction state thereof and supplying said second pulse signal to said second transistor to control the conduction state thereof;

supplying said first complementary signal to said third transistor to control the conduction state thereof and supplying said second complimentary signal to said fourth transistor to control the conduction state thereof; and

controlling the simultaneous conduction of said first and second transistors, and said third and forth transistors, to deliver power to said primary side.

38. A method as claimed in claim 37, further comprising the steps of:

comparing said feedback signal with a reference signal and generating a first output signal based thereon; and

comparing said first output signal with said ramp signal and generating said second pulse signal.

39. A method as claimed in claim 35, further comprising the step of controlling said pulse generator based on a voltage signal across said load.

40. A method as claimed in claim 35, further comprising the step of controlling said pulse generator based on said feedback signal.

41. A method as claimed in claim 35, further comprising the steps of:

supplying a first signal indicative of voltage across said primary said and a second signal indicative of the current through said load to a phase-lock circuit;

locking a phase between said first and second signals and generating a control signal based thereon; and

supplying said control signal to said pulse generator to adjust the pulse width of said pulse signal based on a phase difference between said first and second signals.

42. A method as claimed in claim 37, wherein said step of comparing said first output signal with said ramp signal and generating said second pulse signal further comprises the step of

generating said second pulse signal based on the intersection of said ramp signal and said first output signal.